WHAT IS CLAIMED IS:

1. A thin film transistor substrate for a liquid crystal display comprising:

a transparent insulating substrate;

a thin film transistor on the substrate, the thin film transistor comprising a gate electrode, a drain electrode, a source electrode, a gate insulating layer and a semiconductor layer;

a passivation layer on the thin film transistor opposite the substrate, the passivation layer comprising a flowable insulating material having a groove therein adjacent the thin film transistor;

a black matrix in the groove; and

a pixel electrode connected to the drain electrode.

2. A thin film transistor substrate of claim 1, wherein the passivation layer includes a first contact hole exposing the drain electrode, and the pixel electrode is on the passivation layer and connected to the drain electrode through the first contact hole.

3. A thin film transistor substrate of claim 2, further comprising a storage capacitor electrode on the substrate, wherein the gate insulating layer extends on the storage capacitor electrode opposite the substrate, and wherein the pixel electrode extends on the gate insulating layer, opposite the storage capacitor electrode.

4. A thin film transistor substrate of claim 3, wherein the passivation layer comprises an organic insulating layer.

5. A thin film transistor substrate of claim 4, wherein the dielectric constant of the passivation layer is 2.4 - 3.7.

6. A thin film transistor substrate of claim 3, wherein the black matrix comprises an organic black photoresist.

7. A thin film transistor substrate of claim 6, wherein the surface resistance of the organic black photoresist is equal to or larger than $10^{10}\,\Omega/\square$.

8. A thin film transistor substrate of claim 3, wherein the passivation layer extends onto the gate insulating layer on the storage capacitor electrode.

9. A thin film transistor substrate of claim 8, further comprising a metal pattern on the gate insulating layer on the storage capacitor electrode; and

wherein the gate insulating layer includes a second contact hole exposing the storage capacitor electrode, and the metal pattern is connected to the storage capacitor electrode through the second contact hole.

10. A thin film transistor substrate of claim 8, wherein the passivation layer on the storage capacitor electrode is thinner than remaining portions of

the passivation layer.

11. A thin film transistor substrate of claim 3, wherein the gate insulating layer on the storage capacitor electrode is thinner than remaining portions of the gate insulating layer.

12. A thin film transistor substrate of claim 11, wherein the gate insulating layer comprises two layers having different etch rates, and the gate insulating layer on the storage capacitor electrode comprises only one layer.

13. A thin film transistor substrate of claim 3, further comprising a metal pattern on the storage capacitor electrode and connected to the pixel electrode.

14. A thin film transistor substrate for a liquid crystal display comprising:

a transparent insulating substrate;

a thin film transistor on the substrate, the thin film transistor comprising a gate electrode, a drain electrode, a source electrode, a gate insulating layer and a semiconductor layer;

a passivation layer on the thin film transistor opposite the substrate, the passivation layer having a groove therein adjacent the thin film transistor; and

a black matrix in the groove.

15. A thin film transistor substrate of claim 14, further comprising a pixel electrode connected to the drain electrode, wherein the passivation layer includes a first contact hole exposing the drain electrode, and the pixel electrode is on the passivation layer and connected to the drain electrode through the first contact hole.

16. A thin film transistor substrate of claim 15, further comprising a storage capacitor electrode on the substrate, wherein the gate insulating layer extends on the storage capacitor electrode opposite the substrate, and wherein the pixel electrode extends on the gate insulating layer, opposite the storage capacitor electrode and covered with the gate insulating layer, and lies under the pixel electrode.

17. A thin film transistor substrate of claim 16, wherein the black matrix comprises an organic black photoresist.

18. A thin film transistor substrate of claim 17, wherein the surface resistance of the organic black photoresist is equal to or larger than $10^{10}\Omega/\square$.

19. A thin film transistor substrate for liquid crystal display comprising:

a transparent insulating substrate;

a gate electrode on the substrate;

a gate insulating layer on the gate electrode, the gate insulating layer

comprising an organic insulating material;

a semiconductor layer on the gate insulating layer; and

a source electrode and a drain electrode on the semiconductor layer and spaced apart from one another.

20. A thin film transistor substrate of claim 19, wherein the semiconductor layer comprises amorphous silicon.

21. A thin film transistor substrate according to claim 19 further comprising a silicon nitride layer between the gate insulating layer and the semiconductor layer.

22. A manufacturing method of thin film transistor substrate for a liquid crystal display comprising the steps of:

forming a gate pattern including a gate line and a gate electrode on a transparent insulating substrate;

forming a gate insulating layer on the substrate, including on the gate line and on the gate electrode;

forming a semiconductor layer on the gate insulating layer;

forming a data pattern including a data line which crosses the gate line, a source electrode which is a branch of the data line and a drain electrode;

coating a passivation layer using a flowable insulating material to have a flat surface;

forming a first contact hole which exposes the drain electrode by etching the passivation layer;

forming a pixel electrode on the passivation layer in a region defined by the gate line and the data line;

etching the passivation layer using the pixel electrode as a mask to form a groove; and

forming a black matrix in the groove.

23. A method of claim 22, wherein the passivation layer comprises an organic insulating layer.

24. A method of claim 23, wherein the dielectric constant of the passivation layer is 2.4 - 3.7.

25. A method of claim 22, wherein the black matrix comprises an organic black photoresist.

26. A method of claim 25, wherein the surface resistance of the organic black photoresist is larger than 10^{10} Ω/□.

27. A method of claim 22, further comprising the step of forming a storage capacitor electrode on the substrate under the pixel electrode.

28. A method of claim 27, further comprising the step of etching a portion of the passivation layer on the storage capacitor electrode.

29. A method of claim 28, further comprising the step of etching a portion of the gate insulating layer on the storage capacitor electrode.

30. A method of claim 28, wherein the gate insulating layer has a double-layered structure having a lower layer and an upper layer , and only a portion of the upper layer on the storage capacitor electrode is etched away.

31. A method of claim 27, further comprising the steps of:

forming a metal pattern on a portion of the gate insulating layer on the storage capacitor electrode;

forming a second contact hole in the passivation layer to expose the metal pattern; and

wherein the pixel electrode is connected to the metal pattern through the second contact hole.

32. A method of claim 27, further comprising the steps of:

forming a second contact hole in the gate insulating layer to expose the storage capacitor electrode; and

forming a metal pattern which is connected to the storage capacitor electrode through the second contact hole on the gate insulating layer.

33. A method of claim 22, wherein the gate insulating layer comprises an organic insulating material having a flat surface.

34. A method of claim 33, further comprising the step of forming a silicon nitride layer on the gate insulating layer.

35. A method of claim 34, wherein the silicon nitride layer lies only under the semiconductor layer.

36. A method of claim 35, wherein the semiconductor layer comprises amorphous silicon.

37. A method of claim 22, further comprising the step of forming an etch stopper layer using a photo definable organic material on the semiconductor layer.

38. A method of claim 37, wherein the step of forming an etch stopper layer comprises the steps of:

coating a layer of photo definable material;

exposing to light the layer of the photo definable material from the front side of the substrate using a mask having a pattern of the etch stopper layer; and

developing the layer of the photo definable material to form an etch stopper.

39. A method of claim 38, further comprising the step of exposing to light from the rear side of the substrate before the step of exposing to light from the front side of the substrate.

40. A method of claim 38, further comprising the step of annealing after the step of developing.

41. A method of claim 40, further comprising the step of etching the semiconductor layer using the etch stopper layer as a mask.

42. A manufacturing method of thin film transistor substrate for liquid crystal display comprising the steps of:

forming a gate pattern including a gate line and a gate electrode which is a branch of the gate line on a transparent insulating substrate;

forming a gate insulating layer using a flowable insulating material;

forming a silicon nitride layer on the gate insulating layer;

forming a semiconductor layer on the silicon nitride layer; and

forming a data pattern including a data line which crosses the gate line, a source electrode which is a branch of the data line and a drain electrode.

43. A method of claim 42, wherein the gate insulating layer comprises an organic insulating material.

44. A method of claim 43, wherein the silicon nitride layer lies only under the semiconductor layer.

45. A method of claim 44, wherein the semiconductor layer comprises amorphous silicon.